# V. MINI-DRIFT TUBE (MDT) ELECTRONICS

## *A. Amplifier and Discriminator Board (ADB)*

### A1. Amplifier Discriminator (AD) Channel.

The AD consists of a wide band preamplifier and a fast discriminator with an adjustable threshold. A feature of the proposed design is the differential CMOS current driver at the output. This reduces parasitic feedback to the inputs in comparison to voltage mode drivers, thus increasing amplifier stability.

Two versions of the AD design are proposed. The first version consists of two monolithic chips: an 8-channel preamplifier and an 8-channel discriminator. The second version is implemented in surface mount device (SMD) technology. Both versions of the AD are going through R&D at present, and one of the two will be chosen based on the outcome of a full scale mini-drift chamber prototype test.

The target specifications for the AD are:

| | | |
|---|---|---|
| Amplifier gain (R load = 1 kOm) | - 100 /μA (2x50 mV/μA) | |
| Noise (Cd = 0) at amplifier output | - 50..70 nA RMS | Note 2 |
| Rise time | - < 10 ns | |
| Dynamic range | - 40..60 dB | Note 2 |
| Variable threshold range | - 0.5..5 μA | |
| Output impedance | - high (current driver) | |
| Output signal | - differential 4..5 mA | |
| Power supplies | - ± 5 V | |

Notes:

1. The above specifications may have minor changes after completion of the R&D stage.
2. The worst case values occur for the SMD version and may be improved in the monolithic version.

### A2. ADB Considerations.

We propose that a 32 channel boards be used (one for four eight-wire mini-drift tubes). Each channel can be inhibited at the input of the MDC located in a VME crate in the collision hall. Each 32 channel Amplifier Discriminator Board includes the following parts:

- 32 channels of ADs
- input and output connectors
- a DC voltage controlled test pulser
- low voltage filters
- low voltage fuses
- low voltage indicators (LED)

A 64 channel ADB version is under a consideration and the decision whether or not to use it will be made after this prototype is tested. The ADB should be located a close to the end-plug of drift tubes as possible. The minimum performance required of the ADB is:

- Noise - 100 nA RMS
- Crosstalk between channels - less than - 40 dB

The connection of the electronics to the MDTs should be implemented using short, carefully shielded cables. Complete RF shielding of the tubes is expected to be a part of the mechanical design. For the connection of the ADB outputs to the MDC in the VME crate, 80-conductor high density cable (.025" pitch) will be used. Because of the common gate within one MDC, it is necessary to equalize the length of the cable group going to each MDC, in order to minimize the gate width.

### A3. Low Voltage Supply (LVS).

We propose to use the power supplies currently installed in the muon system. As stated earlier, a bipolar ±5 V supply is needed for the on-chamber electronics. At a power consumption of about 100 mW per channel, the total power will be about 5 kW. If we assume that the muon chamber have an equivalent channel count, then 100 W of LVS power per module is needed. For safe detector operation it is necessary to impose the following condition: the LVS power cables should be able to withstand a short circuit occurring within any part of the on-chamber electronics. Therefore, it is necessary to take the following protective measures:

- implement fuses for each voltage
- the power supplies must have over-voltage protection

To minimize the voltage drop on the power cables, the supplies have to be placed as close to the chamber modules as possible. To monitor the outputs of the LVS, we propose to use the existing Monitor Board [15].

### A4. High Voltage Supply.

We propose to use the 48 eight-channel HV modules currently installed in the present muon system. The mini-drift tube HV supply must deliver up to 5 kV at 2 mA per channel. Each tube will have an individual connector to the HV bus. This allows us to disconnect an individual tube (8 channels) in case of any HV problems.

### A5. Slow Monitoring.

We propose to use the existing muon Monitor Boards (MB) to measure LVS voltage and current, chamber gas flow, pressure etc. Each MB has input and output registers, a scanning ADC and multi-channel DAC etc. This monitoring is necessary for the safe and reliable operation of the detector. The list of parameters to be monitored includes:

- output voltages of the LVS
- gas flow
- gas pressure
- temperature at a few points around the system

The parameters of the HV power supply such as individual voltages and current limits will be controlled by the existing CDAQ system [16].

### A6. Timing.

The D0 muon system in Run II operates synchronously with the main Tevatron frequency of 53 MHz [17]. To define the timing of the readout electronics the following values must be considered:

| | |
|---|---|
| minimum bunch crossing interval | - 132 ns |
| maximum drift time | - 60 ns |
| maximum propagation delay along a 6 meter tube | - 20 ns |
| differences in arrival times for 192 channels in one octant | - 5 ns |

Based on the sum of all the contributions to the difference between signal arrival time and bunch crossing, the gate width in the MDC should be no longer than 90 ns.

### A7. Surface Mount ADB Version.

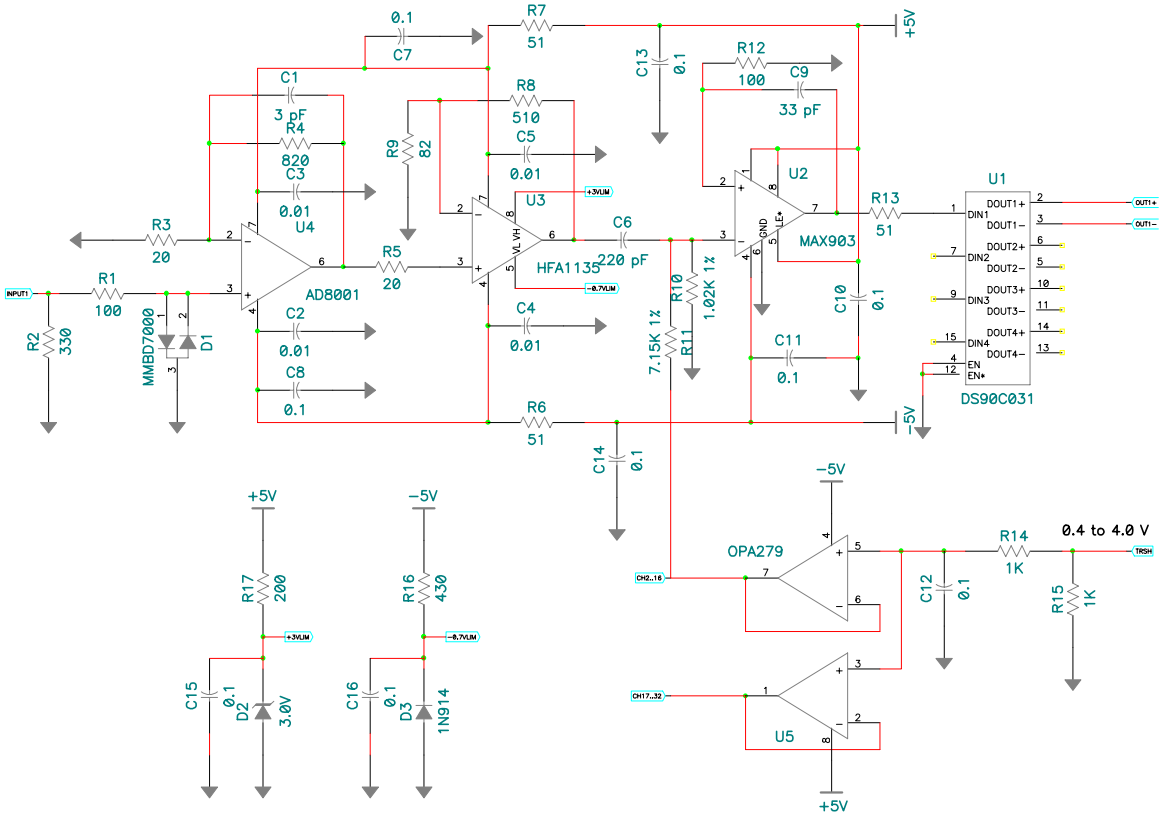



Fig. V-1. One channel SMD Amplifier-Discriminator.

A schematic diagram of the SMD version of the AD is presented in the Fig. V-1. It uses commercially available amplifiers (Analog Devices AD8001 and Harris HFA1135A)) and a commercial discriminator (MAXIM MAX903). A CMOS LVDS level current mode

output driver (National DS90C031) is used. The circuit has a good stability and noise performance, and wide bandwidth.

A test signal supplied by the MDC fires a on-board test pulser. The amplitude of the pulser is controlled by an analog voltage from the MDC. All the channels of one ADB are fired simultaneously.

### A8. Monolithic ADB Design.

An eight channel current amplifier/shaper(Ampl-8) and an eight channel discriminator (Disc-8) having the common designation D0M ("Dubna+D0+Minsk") have been designed as an R&D project for the D0 Muon Electronics Upgrade. A pilot batch (10 wafers) was produced in February, 1997. The chips were packaged and measured. On the basis of initial measurement results, the second iteration of the design is now in progress. Only minor corrections have made to the discriminator circuit. In the current amplifier chip the reference points for the common base amplifier stages have been brought out to external pins. The output offsets can now be corrected by external Op-amp based feedback. In addition, a new cascode-based current amplifier version has been designed and put into production.

A special aluminum package has been designed and produced for the ICs. A 32-channel PCB has been designed and is in production.

### A9. The BiFET Technology.

This design is implemented in a BiFET process [18] with the following features:

- Only npn transistors and p-channel JFETs are used
- The presence of two buried layers ($n^+$ and $p^+$) within n-type epitaxial structures
- Combined isoplanar oxide isolation
- Self-aligned $n^+$ gate and n+ emitter structures
- Ion implantation only
- Boron doping through a preliminary grown thermal oxide
- Simultaneous forming of different conductivity type regions
- 14 photolithography operations, eight block structured doping steps
- Two-level metallization

The npn transistors have $f_T$ = 3GHz and $\beta \approx 80$. The low power version of the p-channel FETs have $f_T$ = 300MHz. and can be placed in any part of a chip. This process has proven to be neutron radiation tolerant [19].

### A10. The Current Amplifier.

#### a) The amplifier circuit

The AMPL-8 (See Fig. V-2) consists of a common base/common collector configuration input stage (*Q1, R2, Q2, Q21, ree*), two differential voltage amplifier stages

(*Q3, Q4, R2C1, R2C, Q6, R2E* and *Q10, Q11, R3C1, R3C2, Q12, R3E*, respectively), two output emitter followers (*Q14, Q17, ROUT2 and Q13, Q16, ROUT1*, respectively), and a bias voltage generating structure attached to the first of the two differential amplifiers (*Q501, R502, R503, Q502, Q527, ree5*).

The common-base input circuit *Q1, R3* uses a low-noise UHF npn transistor ($R_{bb'} \leq$ 30Ohm, $f_T >$ 3GHz). The common-base configuration operates at a large collector current to provide a low input impedance over a wide frequency range. The amplifier input is protected from positive (*Q1001*) and negative (a chain of two large-area diodes, *Q2001, Q3001*) overvoltage pulses. This stage converts input current to voltage across resistor *R2.* The differential stages provide the necessary voltage gain. The emitter followers *Q5, Q9* and *Q15, Q18* with matched diode chains perform coupling with level shifting between the stages, and the emitter followers *Q14, Q17,* and *Q13, Q16* provide the required output drive capacity.

The structure used to establish the base potential of *Q4* is a common base/common collector stage (*Q501, R502, R503, Q502, Q527, ree5*), which is similar to the input stage but having collector currents exactly ten times smaller.

Signal shaping is provided by the differential stage transistors' *(Q3, Q4, Q10, Q11*) collector capacitance and their loading resistors (R2C1, R2C, R3C1, R3C2).

b) The amplifier layout

The layout of one channel of AMPL-8 (Fig. V-3) has the following features:

- The layout is 320 μ wide and is set by the geometry of the bonding pads
- Each channel is shielded by a contact to the substrate which is connected by a metal trace to a separate contact pad (SUB) having no connection to a supply line
- Each Ampl-8 channel has diode voltage protection against positive and negative overvoltage pulses which adds 8.52pF to the input capacitance. All protective diodes of both polarities consist of two sections, making it possible to reduce the capacitance by half at the cost of 50% reduction of the diode area with a corresponding decrease in overcurrent capacity
- Each input of the Ampl-8 channel has a separate ground line PGND originating at the input transistor base, which are not connected to ground inside the chip
- The eight channels have a common ground line VGND which ties the collectors of the *Q7*s of all the channels. By varying the value of an external resistor $R_{ext}$ connected to this point and a fixed positive supply voltage or connecting a fixed resistor to an adjustable voltage, one can regulate the standing current of all the Ampl-8 transistors except the input transistors *Q1, Q501*

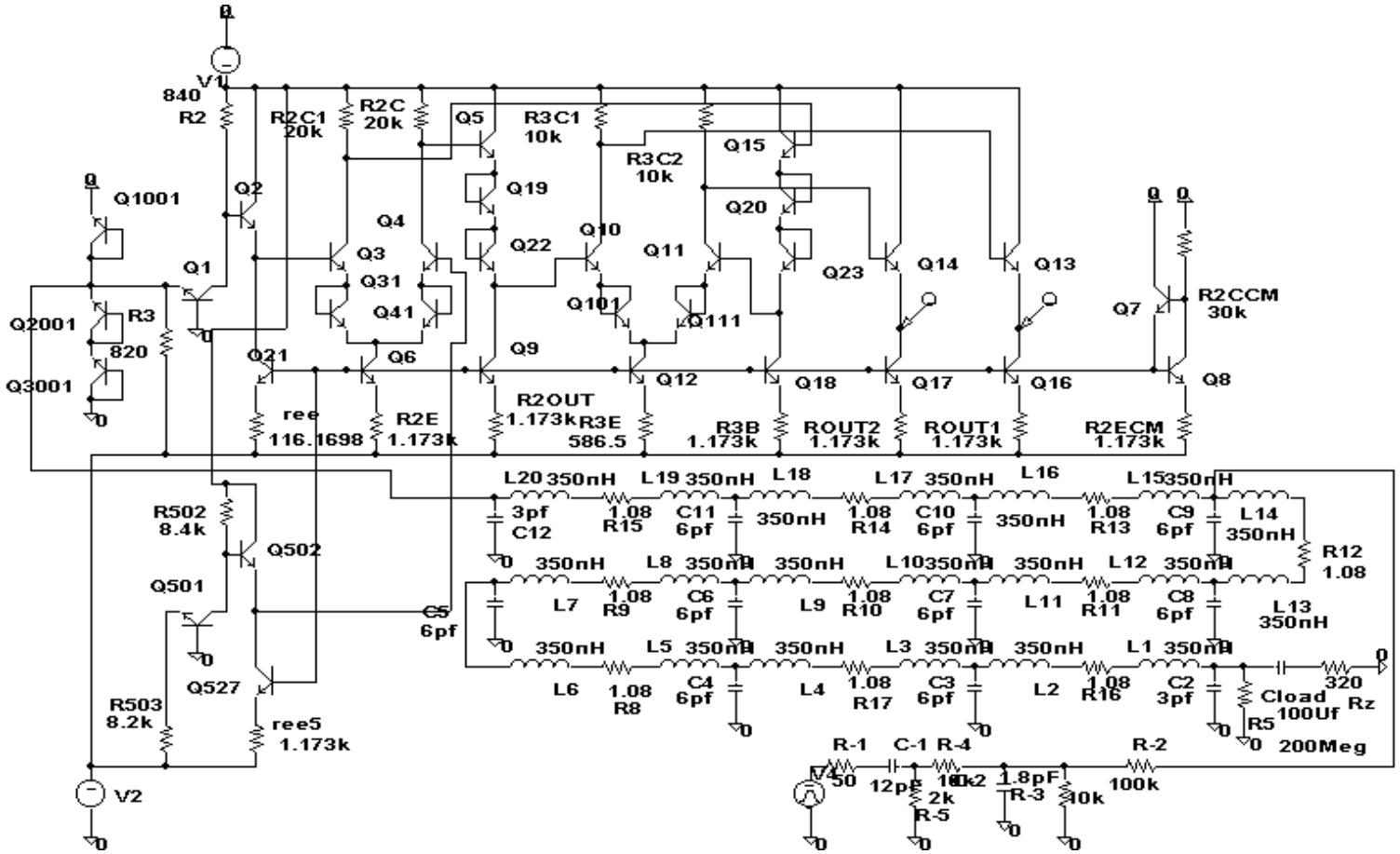



Fig. V-2. The current amplifier circuit.

- There are separate contact pads tied to a substrate in the Ampl-8 and Disc-8 which have no connections to the negative supply. Applying a large negative potential limited by the breakdown voltage to the substrate, one can substantially decrease the capacitance between the internal structures and the substrate, i.e. interelement and interchannel coupling

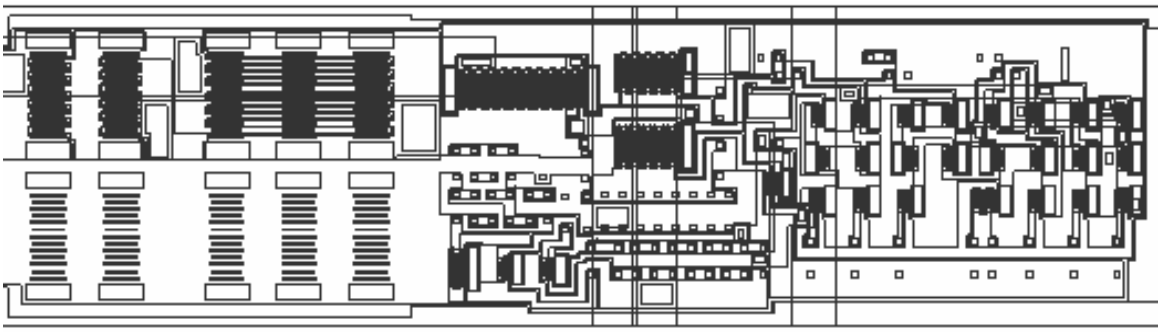


Fig. V-3. The single channel current amplifier layout.

c) Measurement results

The Ampl-8 amplifiers were bench tested. The detector capacitance was simulated by a 60cm length of 50 Ω cable with a capacitance of 60 pF. The input signal (Fig. V-4) was simulated by the RC-circuit shown in Fig. V-2 at the input of the amplifier between a pulse generator and a long transmission line.

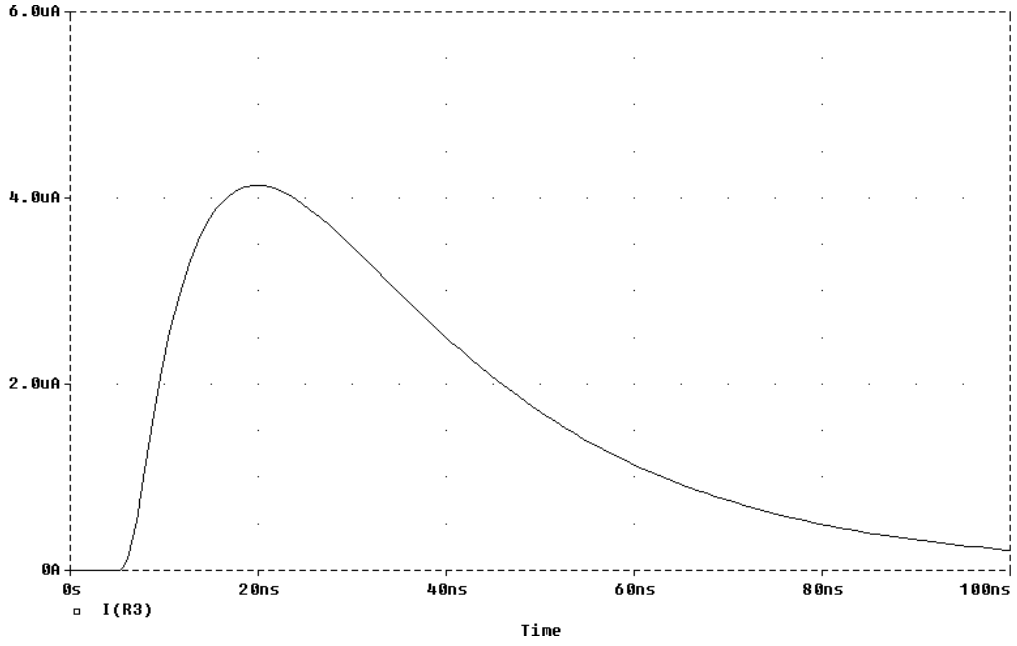



Fig. V-4. Test signal waveform.

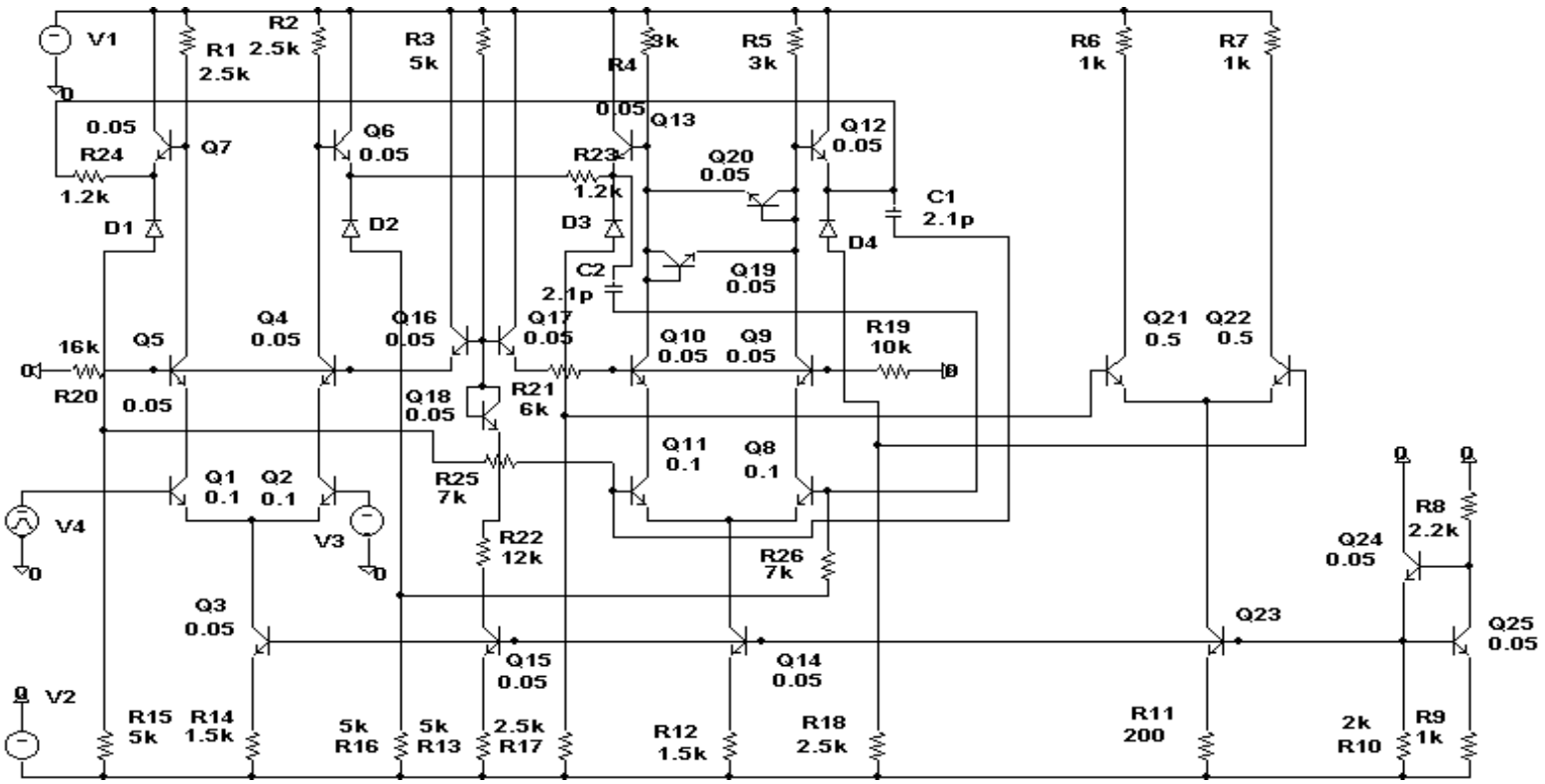



Fig. V-5. The circuit of the discriminator DISC-8 version 1.

The simulated and measured characteristics of the current amplifier AMPL-8 are shown in Table V-1.

Table V-1. Current amplifier specification

| Parameters | Predicted value | Measured value |
|---|---|---|
| Current gain | 100 mV/μA (50 mV/μA per arm) (Note 1) | |
| ENC for detector capacitance:<br>$\tilde{N}^d$ = 0, r.m.s. electrons,<br>$\tilde{N}_d$ = 60 pF, r.m.s. electrons, | <br>4000<br>8000 | <br>not measured<br>≤13800 |
| Output signal leading edge | 5-7 | 8 |
| Input dinamical range, dB | 60 | |
| Input signal polarity | ± | ± |
| Input impedance, Ω | 10 | ≤10 |
| ± overvoltage protection | Yes | Yes |
| Channel number | 8 | 8 |
| Input linear range | 40 | |
| Differential output | Yes | Yes |
| Available output load, Ω | 50-2000 | |
| Cross-talks, dB | -46 | |
| Voltage supply, V | ±5 | ±5 |
| Dissipated power, mW/channel | (Note 2) | 75 |
| Package | To be chosen | Custom QFP-48-1.27 |

Note 1: When loaded by 1 kΩ at the comparator input
Note 2: To be minimized.

## A11. The Discriminator.

### a) The discriminator circuit

The discriminator consists of eight parallel channels having common voltage supply lines and a common output current control. There are no built-in threshold control circuits inside the IC. An open collector output has a compliance from 0 V to 5 V and can thus be made compatible with ECL, NIM, and TTL depending on the supply voltage.

A circuit diagram of a single channel is shown in Fig. V-5. The discriminator has three differential stages, the first and the second (with a resistor load) provide the voltage amplification required, the third (with open collector) has an internal load. The comparator has a differential input and a complementary current output. The first differential stage Q1, Q2 is loaded by the common base stages Q4, Q5 to decrease their Miller capacitance and dependence on input capacitance. The second differential stage has a similar structure. The back-to-back diodes Q19, Q20 limit the maximum voltage between the collectors of Q9, Q10 thus increasing speed. The emitter followers Q6,

Q7, Q12, and Q13 with matched Zener diodes D1-D4 provide level shifting and coupling between the differential stages. The second differential stage has a feedback network comprised of resistors R23, R24, R25, R26 and C1, C2. This networks limits the output pulse width to 60 ns. The traces of R8 from each channel are tied together and brought out to separate pin VGND, permitting the control of the output current by changing the voltage at this pin or by varying R8.

b) The discriminator layout

The layout of one channel of the discriminator is shown in Fig. V-6. The dimensions of one discriminator channel without contact pads is 320μ x 770μ, and the area of the 8-channel discriminator die with contact pads is 1.1 x2.9 mm. The channel width is determined by the minimum size of the contact pads (100μ) and admissible gaps between them (60 μ). It should be noted that both Ampl-8 and Disc-8 have the same width, which makes it possible in future to fabricate them as a single 3.3 x 2.3 mm amplifier/discriminator chip (along with test structures, identifier marks etc.).

The layout of the comparator has the following features:

- Each channel is shielded by a contact to a substrate, which is connected by a trace to a separate contact pad (SUB) having no connection to a supply voltage
- The zero potential line (GND) has two contact pads connected in parallel
- The Zener diodes are comprised of a reverse biased emitter junction of a npn transistor with the collector tied to the positive supply
- To decrease the capacitance at the collectors of Q9 and Q10, the back-to-back diodes Q19 and Q20 have been made with an additional p-area formed in the epitaxial well of the npn transistor.

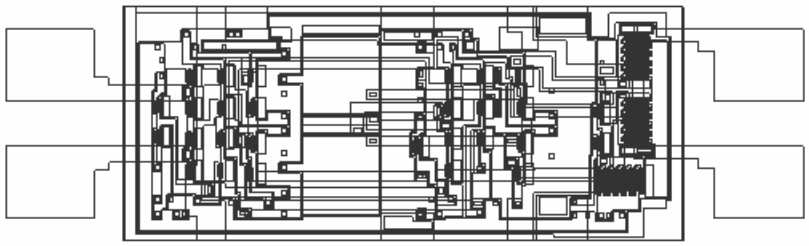


Fig. V-6. The discriminator v.1 single channel layout.

c) Testing and Results

To test the chip, a probe card was designed which contains an eight channel zero-crossing discriminator. The measured parameters of this discriminator are shown in

Table V-2. The chip has satisfactory speed: the rise and fall times are 1.8 ns and 2.2 ns respectively when operated with a 110 Ω load. Channel to channel variation of the propagation delay is less than 4 ns. The output is designed to emulate a DS90C031 differential line driver connected to 20 m of ribbon cable. The power dissipation is 84 mW per channel.

Table V-2. Specifications of the eight-channel comparator IC

| Parameter | Value |
|---|---|
| Supply voltage, V | +5, -5 |
| Supply current $I^+$, $I^-$, mA | ≤65, ≤69 |
| Supply current $I^+$, $I^-$/chan, mA | ≤8.2, ≤8.6 |
| No. of channels | 8 |
| Offset, mV | ≤ |
| Output current, mA | ≤4 |
| Input differential bias current, μA | ≤0.01 |
| Input bias current, μA | ≤1 |
| Propagation delay at 10 mV/60 mV, ns | ≤36, 14 |
| Output rise/fall times, ns | 2.2 / 1.8 |
| Maximum propagation delay difference, ns | ≤4 |

The dependence of propagation delay on overdrive is shown in Fig. V-7.

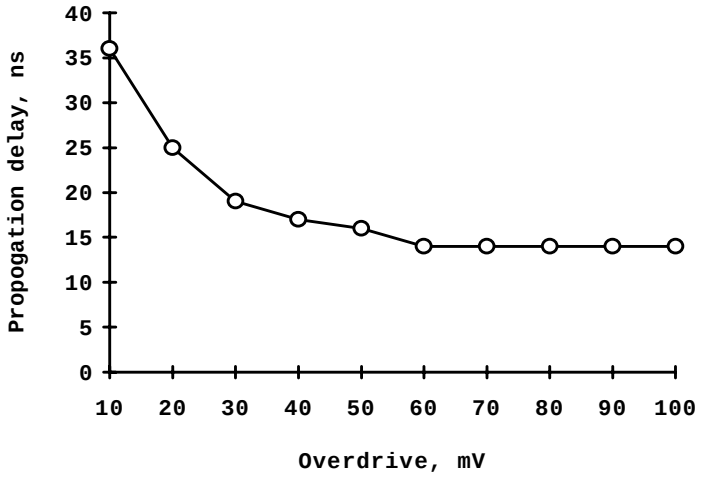



Fig. V-7. The dependence of propagation delay on overdrive.

Time walk was measured to be 3.8 ns for input overdrives of 20 mV and 100 mV ($2Q_{th}$ and $10\ Q_{th}$) at a threshold corresponding to an amplifier input current of 0.5 μA.

## A12. The Second Iteration of the Design.

### a) Contents of the second iteration

While fabrication of the wafers for the first iteration was in progress, a design for a second batch of wafers was started, but interrupted before metallization. New photomasks

for the metal layers were made, in order to modify the amplifier and discriminator circuits according to the test results from the first iteration. We have put into production two versions of the current amplifier, AMPL-8 v.2 with common base input stages and new AMPL-8 v.3 with cascode input stages, and one version of the discriminator, DISC-8 v.2.

b) AMPL-8 v.2 (common-base)

A common base stage with an additional input connected to the reference stage input transistor base to balance the amplifier's differential outputs with an external Op-amp for each channel has been designed. A Pspice simulation has confirmed the operation of this version. When this approach is validated my measurement performed on the chips, the Op-amps will be integrated onto the chip. The base of the input transistor is connected to the collector of Q7 (these points on all channels are tied to the VGND pin) inside the chip thereby providing the possibility of connecting the amplifier inputs directly to the detectors by separated two-wire lines to minimize possible cross talk. The AMPL-8 v.2 layout is shown on Fig. V-8.

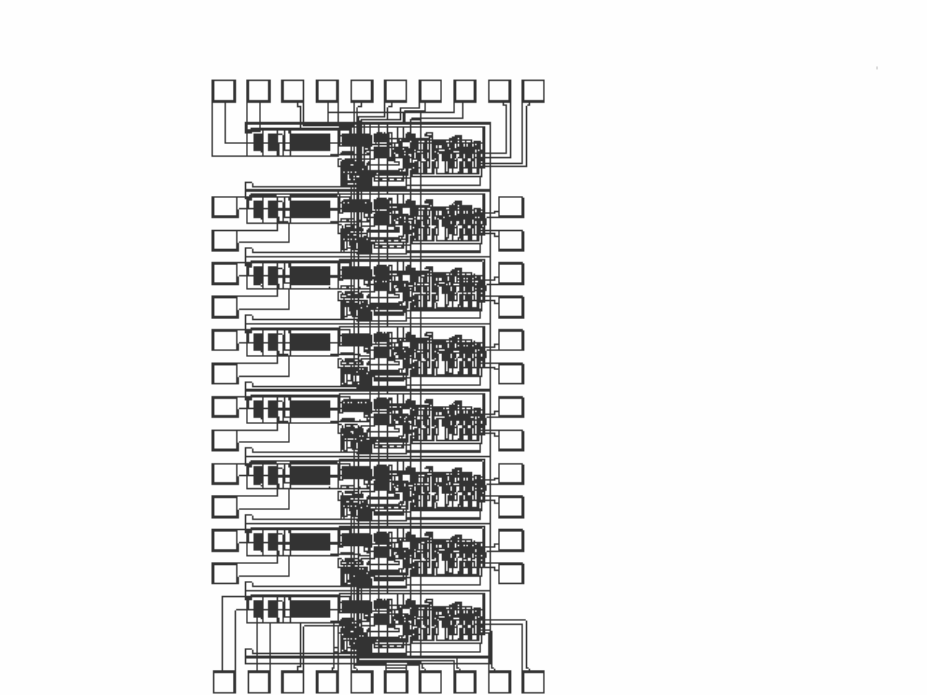


Fig. V-8. The layout of AMPL-8 v.2 (common base).

c) DISC-8 v.2

A modification to the basic discriminator circuit (Fig. V-5) is an additional output from R8 for separate control of the current mirror, permitting adjustment of the output stage standing current over a ±20% range. The remander of the circuit is unmodified.

A13. Packaging.

The ICs are encapsulated in a 48-pin four-side planar package. The package has been specially designed for the D0M Ampl-8 and Disc-8. It consists of an aluminum base, a

covar leaded chip carrier (mounting pad), and a covar grounded cover. The package pinouts for the chips are shown in Fig. V-9, Fig. V-10, and Fig. V-11.

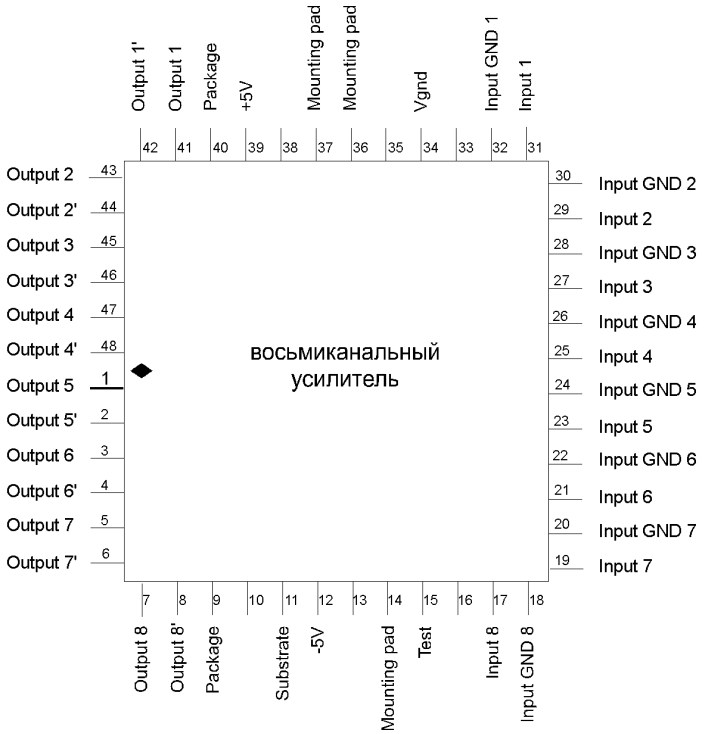



Fig. V-9. The Pinouts for AMPL-8 version 1

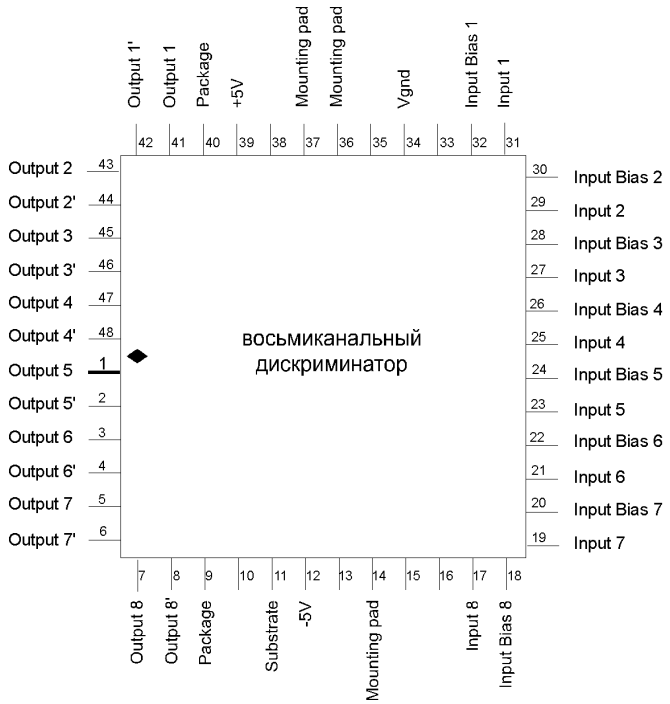



Fig. V-10. The Pinouts for DISC-8 version 2

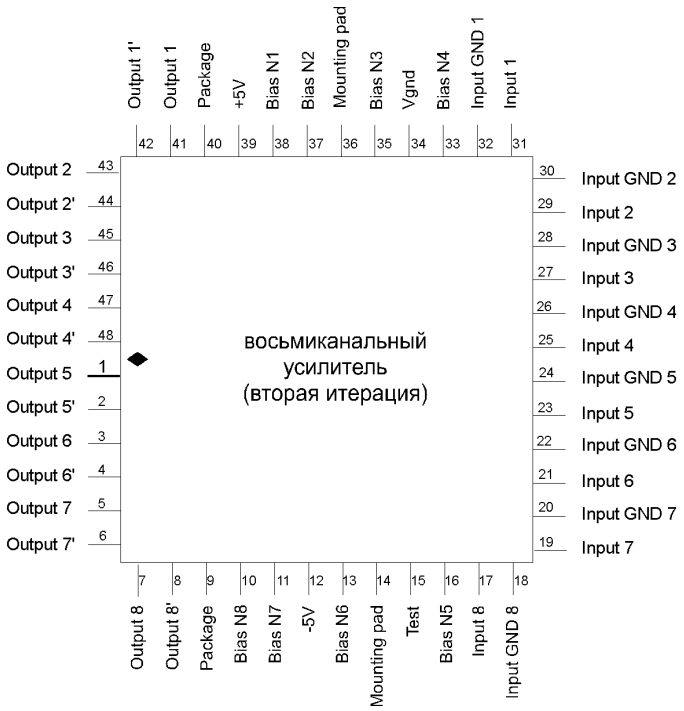



Fig. V-11. The Pinouts for AMPL-8 version 2

## *B. Mini-Drift Tube Digitizing Card (MDC)*

### B1. Introduction

The Mini-drift tube Digitizing Card (MDC) is a part of the D0 Muon Mini-Drift Tube Chamber Electronics [6]. The Mini-Drift Tube (MDT) Chamber Electronics includes on-chamber Amplifier-Discriminator Boards (ADB), MDC and Mini-Drift Tube Readout Controller (MDRC). The MDC and MDRC are housed in 9U VME crates located on the detector platform. The primary functions of the MDC modules are Level 1 trigger hit bit generation and coarse time measurements of the drift time within the specified gate width. The design of the MDC implements the following features:

- reception of 192 discriminator signals from the Amplifier-Discriminator Boards
- digitization of the arrival time of the input signals within a preset gate interval
- transmission of the latched hit bits to the Level 1 trigger system via high speed serial links
- fixed event output data format as nine 64-bit words
- two analog control signals, Discriminator Level and Test Pulse Level, to control on-chamber electronics
- test signal to fire the ADB's on-board pulser

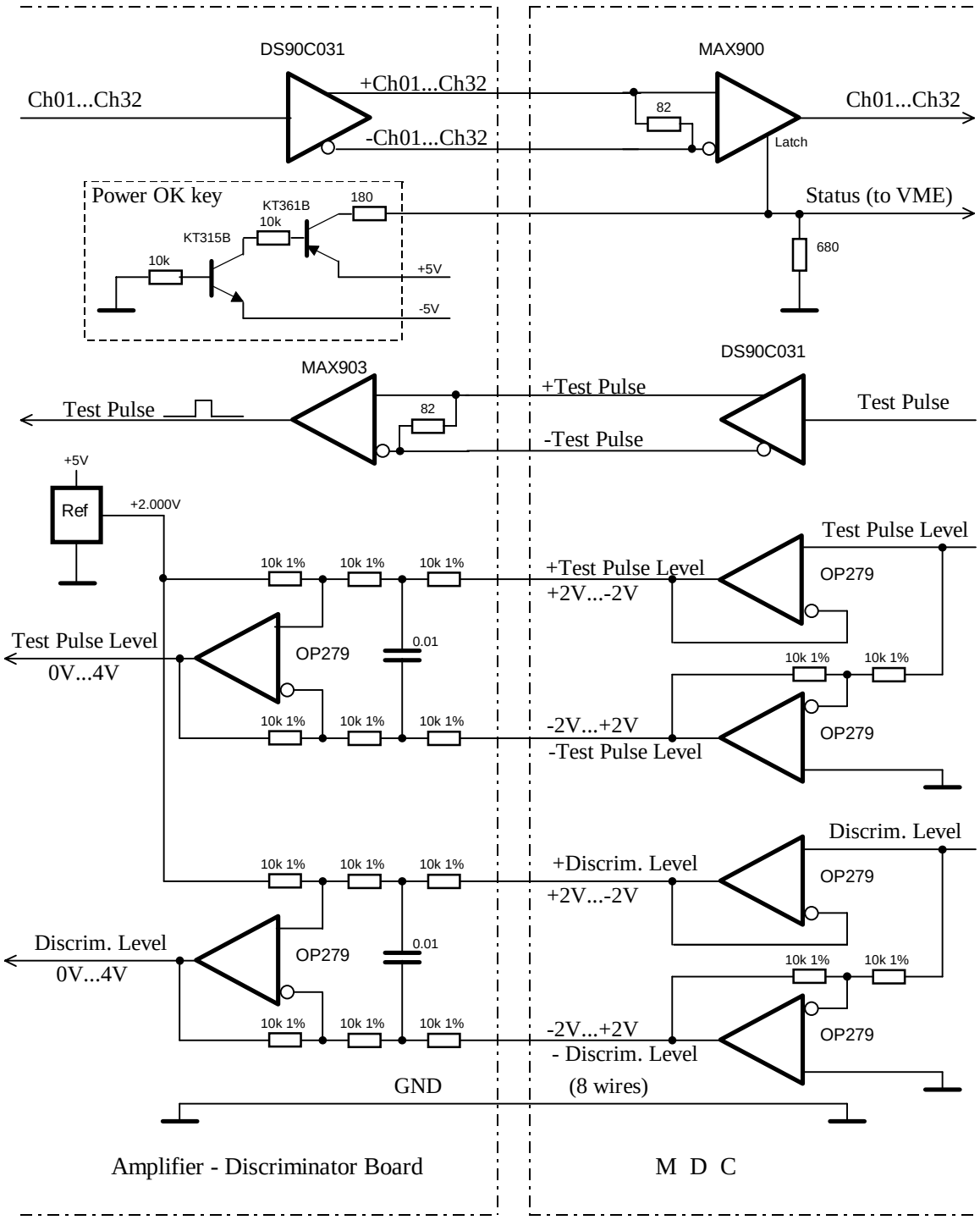



Fig. V-12 ADB to MDC connection.

- programmable test signal for internal testing
- mask register for 192 channels to provide selective channel enables
- front panel 192-channel OR output with an LED indicator for debugging and self-triggering

- three front panel LEDs to indicate VME access, MDRC readout access and Power OK

### B2. Mechanical Specification

The MDT Chamber Electronics is based on VME 9U crates widely used in D0. It is assumed that each MDT crate constitutes a stand-alone readout station within the D0 detector and therefore has to have an individual AC outlet available on the platform. The MDC is implemented as 9U by 280 mm VME card. The MDC uses three backplane connectors (see Appendix B) for the following functions:

- **J1/J2** connections for standard VME operations
- custom **J3** connections for fast 64-bit wide data readout and for timing & control signals.

There are six 80 pin high density connectors located on the front edge of the MDC to provide connections for the Amplifier-Discriminator Boards (32 channels per connector). Two HF connectors bring out two high-speed serial links from the Serial Transmitter Daughter Boards [12] (STDB) designed by Arizona University. An OR output signal uses a LEMO connector with an associated LED indicator. Three more LEDs indicate VME and MDRC readout access to the module and Power OK status.

### B3. ADB to MDC Interconnection

The Amplifier-Discriminator Board transmits data signals using the National DS90C031 LVDS - Low Voltage Differential current line drivers with a +/- 330mV swing. A high density 0.025” pitch 80 conductor cable is used to deliver signals from the ADB to MDC. Cable pin assignment is shown in Table V-5, Appendix B, and Fig. V-12 gives an example of this connection. It is assumed that all signals on all six cables arrive with equal delays, hence there is no need for individual channel-by-channel delay adjustment within the MDC. Each differential line is terminated with a single 82 **Ω** resistor. The MAX900 comparator translates the differential input signal to a TTL level. To prevent oscillations, an additional wire brings a TTL level to the latch input of the comparator. When the input cable is disconnected or the ADB power supply is turned off, the output of the comparator is latched thus inhibiting oscillations. In addition, two analog differential signals and one logical differential signal are sent to the ADB to control the discriminator thresholds and test pulser.

### B4. Other Output Signals

Each MDC module uses two STDBs to provide hit information to the Level 1 trigger system. The STDB is arranged as a separate daughter board and has a parallel 16-bit input and HF output coaxial connector. The daughter board is synchronized to the accelerator RF (53 MHz) and is capable of transferring 96 bits of information within a 132 ns interval. The Level 1 trigger bit data format is shown in Table V-6.

The front panel Fast OR output provides an OR from all 192 channels, Fig. V-15. The Fast OR signal available on the J3 backplane also. Each output pulse is accompanied by a

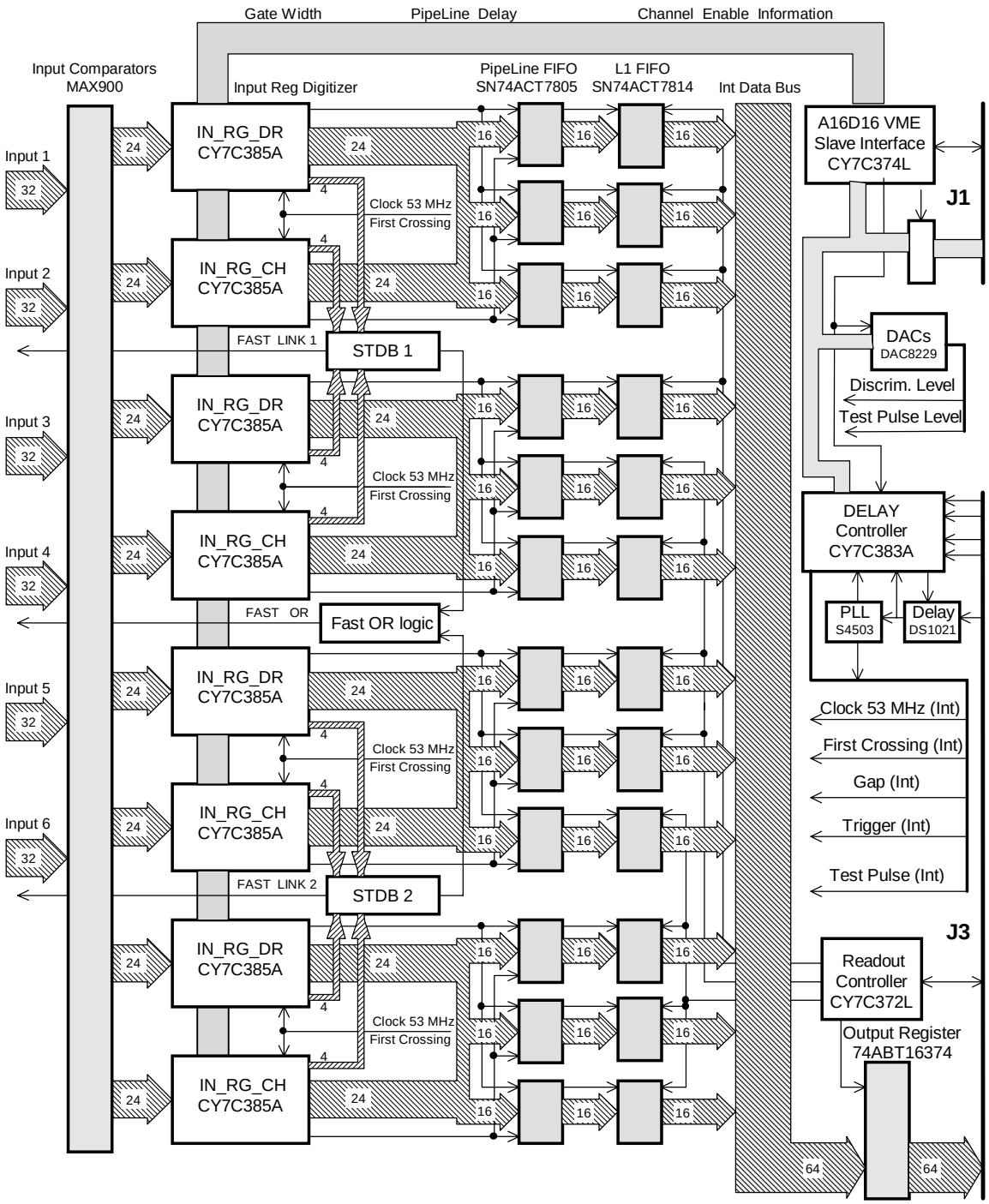



Fig. V-13. MDC block-diagram.

20 ms long flash of its LED indicator. The primary purpose of the outputs is to provide a simple tool for testing and debugging as well as a signal source for local triggering.

## B5. Signal Processing

The MDC module is designed to run synchronously with the accelerator RF clock frequency of 53.104 MHz. The MDRC receives encoded timing signals from the MRC, decodes it, and fanouts to the MDCs. The timing signals include RF, First Crossing (FC)

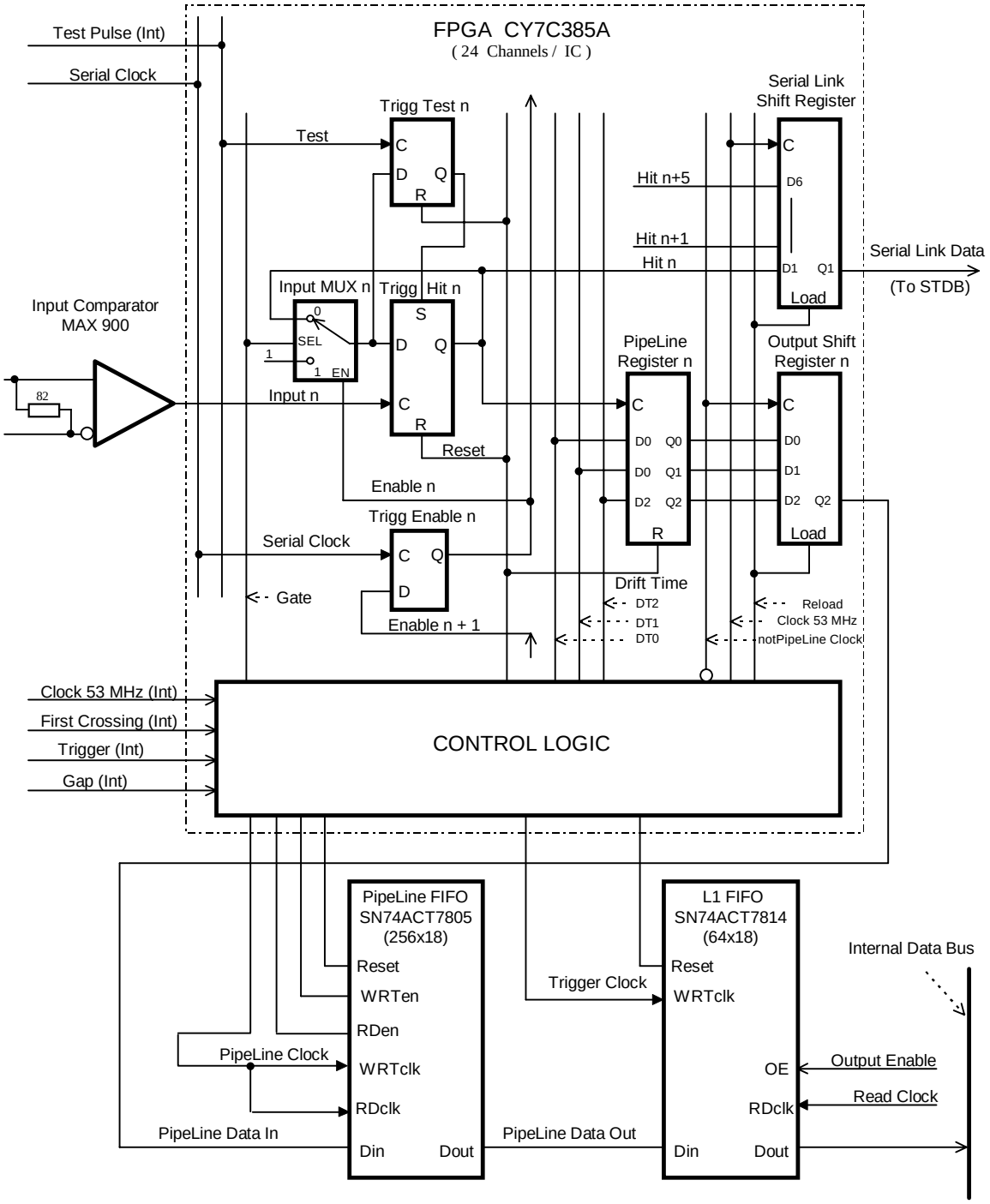



Fig. V-14 MDC data channel block-diagram.

and Sync Gap (SGap). The FC signal marks the bunch crossing in the detector as crossing number one, while SGap controls the transmission of data to the L1 trigger system. The MDRC drives the MDC with an RF/7 reference frequency and the MDC recovers the RF clock of 53.104MHz using an AMCC S4503 Clock Synthesizer circuit. The rest of the control signals are generated locally.

All signal processing functions are implemented in a Cypress CY7C385A FPGA chip. Each FPGA contains the logic for 24 individual channels (Fig. V-14). The MDC accepts

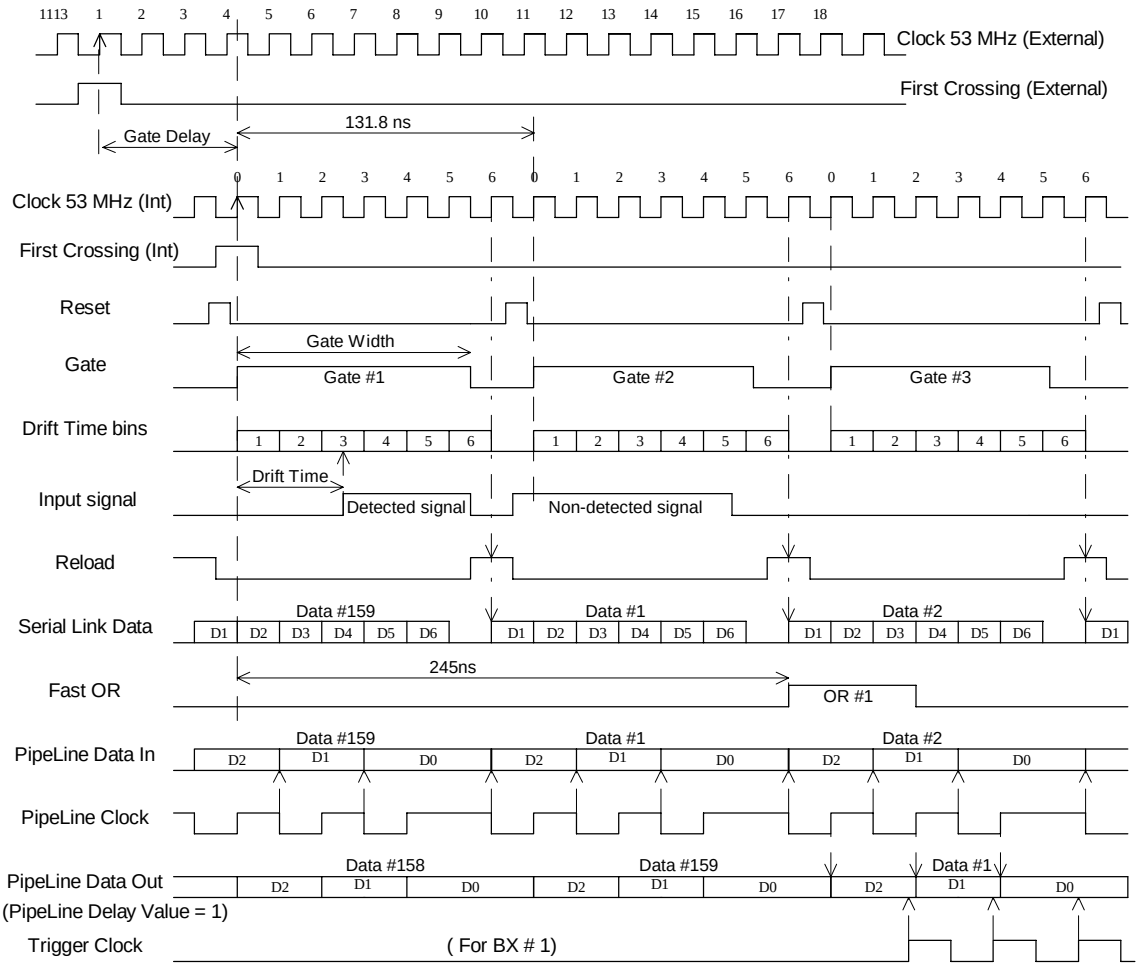



Fig. V-15 MDC timing diagram.

asynchronous discriminator signals from the ADB and stores them in an input D-type flip-flop (Trigger Hit) coincident with the Gate and Enable signals. The Gate signal is common for all channels while the Enable signal is individual to each channel and can be downloaded (Appendix C). The stored bits are then reloaded into the Serial Link Shift Register and shifted outside the FPGA chip to the Serial Link Daughter Board at the RF clock frequency.

When Trigger Hit is set, the current value of the Drift Time bus is loaded to the Pipeline Register. At the end of the Gate signal the Drift Time value, saved in the Pipeline Register, is transferred to the Output Shift Register and shifted out of the FPGA to the Pipeline FIFO. If Trigger Hit has not been set during the gate period, a zero value is stored in the pipeline. If the Trigger Hit was set, a corresponding drift time value (1..6) is stored in the pipeline. Gray coding is used to limit metastability related errors to one LSB. A simplified MDC timing diagram is shown in Fig. V-15 [22]. The Pipeline FIFO is used to delay the incoming data stream for a fixed period of time, until the corresponding L1 Accept signal is received (about 4.2μs). The Pipeline FIFO is based on a Texas Instrument SN74ACT7805 clocked FIFO (256 x 18 bit). All control signals are generated within the FPGA. The Pipeline Delay (PD) value is programmable (Appendix C) and has to be downloaded during the initialization procedure. When an L1 Accept signal arrives, the

data from the appropriate crossing is supposed to be present at the pipeline output. The FPGA generates a Trigger Clock signal to load data to the L1 FIFO. The data saved in the L1 FIFO is ready to be read out by the Readout Controller. The data path is deadtimeless, as next L1 Accept can be processed immediately and next data block will be saved in the L1 FIFO. The maximum storage capacity of the FIFO is 21 events. L1 FIFO is based on a Texas Instrument SN74ACT7814 strobed FIFO (64 x 18 bit).

### B6. Data Readout Interface

A simple interface is used for sequential data transmission to Readout Controller card. Data is transferred over a 64-bit wide Data Bus at a 10 MHz or 80 Mbytes/s transmission rate (Fig. V-16). This provides a 100ns * 9 = 900 ns readout time per MDC. Each MDC module is addressed using a 4-bit readout Address Bus which is set by the lowest order portion of the VME address DIP switch. Up to 15 MDCs per crate can be addressed.

The Data Readout Interface uses J3 connections and is based on SN74ABT16374A and SN75ABT16821 TTL data transceivers. The timing and control signals occupy several lines of the same J3 connector (Table V-9). The Readout Interface pin assignments are shown in Table V-9, Appendix B.

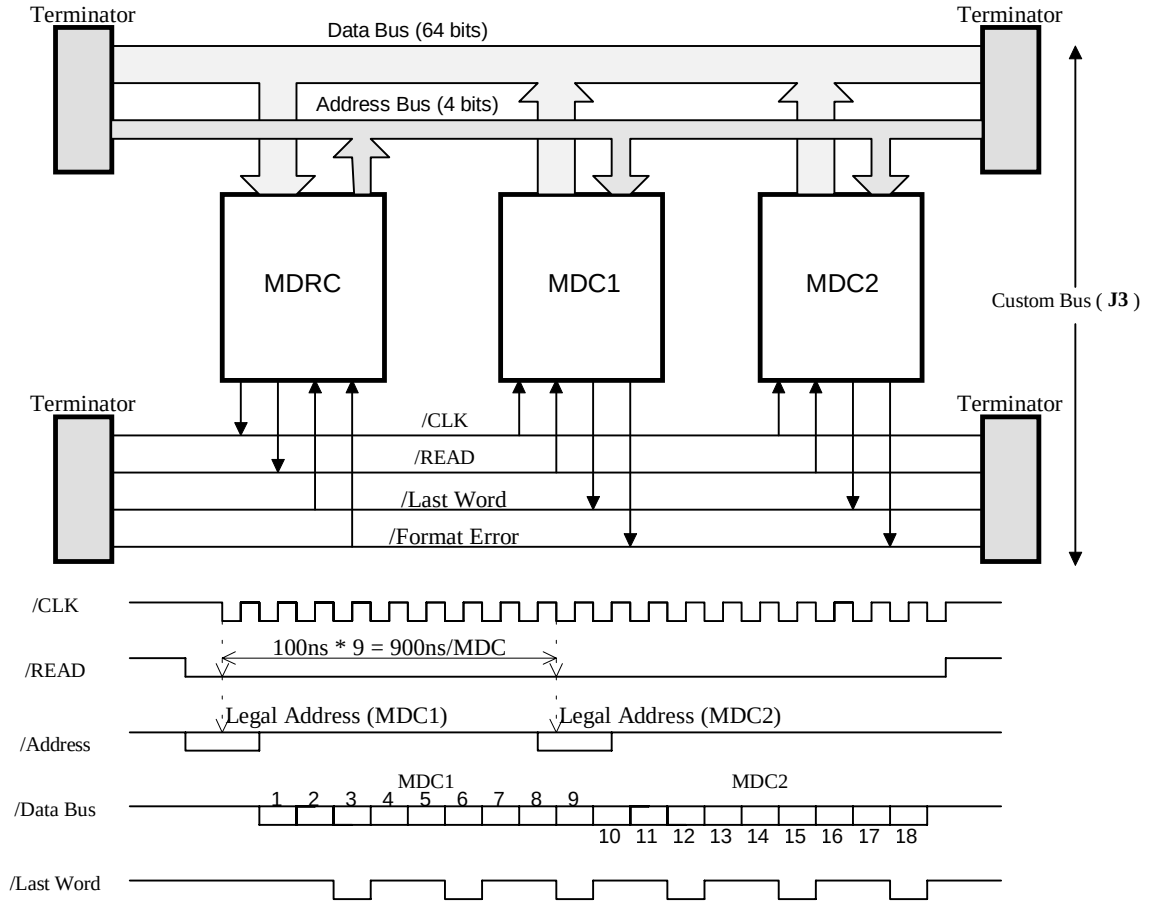



Fig. V-16 MDC data readout interface & timing.

The data readout interface output data format is shown below in Table V-3. The Gray code drift time bits D2, D1, D0 are shown in Table V-4.

Table V-3 MDC Output Data Format.

| Data Lines: D_xx | 64 | 63 | 62 | 61 | - | | - | 02 | 01 |
|---|---|---|---|---|---|---|---|---|---|
| Channel number | 064 | 063 | 062 | 061 | - | | - | 002 | 001 |
| Word 1 | D2 | D2 | D2 | D2 | - | | - | D2 | D2 |
| Word 2 | D1 | D1 | D1 | D1 | - | | - | D1 | D1 |
| Word 3 | D0 | D0 | D0 | D0 | - | | - | D0 | D0 |
| Channel number | 128 | 127 | 126 | 125 | - | | - | 066 | 065 |
| Word 4 | D2 | D2 | D2 | D2 | - | | - | D2 | D2 |
| Word 5 | D1 | D1 | D1 | D1 | - | | - | D1 | D1 |
| Word 6 | D0 | D0 | D0 | D0 | - | | - | D0 | D0 |
| Channel number | 192 | 191 | 190 | 189 | - | | - | 130 | 129 |
| Word 7 | D2 | D2 | D2 | D2 | - | | - | D2 | D2 |
| Word 8 | D1 | D1 | D1 | D1 | - | | - | D1 | D1 |
| Word 9 | D0 | D0 | D0 | D0 | - | | - | D0 | D0 |

Table V-4 Drift Time Bit Assignment.

| D2 | D1 | D0 | Time bin |
|---|---|---|---|
| 0 | 0 | 0 | No Hit |
| 0 | 0 | 1 | Bin 1 |
| 0 | 1 | 1 | Bin 2 |
| 0 | 1 | 0 | Bin 3 |
| 1 | 1 | 0 | Bin 4 |
| 1 | 0 | 0 | Bin 5 |
| 1 | 0 | 1 | Bin 6 |
| 1 | 1 | 1 | Illegal |

## B7. VME Interface

The main purpose of the VME interface is to provide a read/write path for control and status information. The digitized hit information is inaccessible from VME and can only be read out by the MDRC. The MDC uses a standard Short I/O A16:D16 Slave Interface. An eight bit DIP switch sets the base address compared to the A05..A12 address lines. The remaining most significant bits of the address (A13..A15) should be set to zero. One MDC uses 16 contiguous addresses. The description of the control and status registers is listed in Appendix C. Only eight of sixteen addresses are actually used in the current design. The remaining addresses are reserved for future expansion.

The VME interface pin assignments are shown in Table V-7 and Table V-8, Appendix B.

## *C. Mini-Drift Tube Readout Controller (MDRC)*

### C1. Introduction

The Mini-Drift Tube Readout Controller (MDRC) is a part of the D0 Muon Mini-Drift Tube Chamber Electronics [6]. A block-diagram of the MDT front-end crate is shown in Fig. V-17. Each crate contains up to 15 MDCs, an MDRC and a VME Master. The MDCs running under the control of the MDRC are continuously digitizing ADB data and sending raw hit information to the L1 Trigger. The MDRC is responsible for submitting L2 and L3 Data upon request of the TFW.

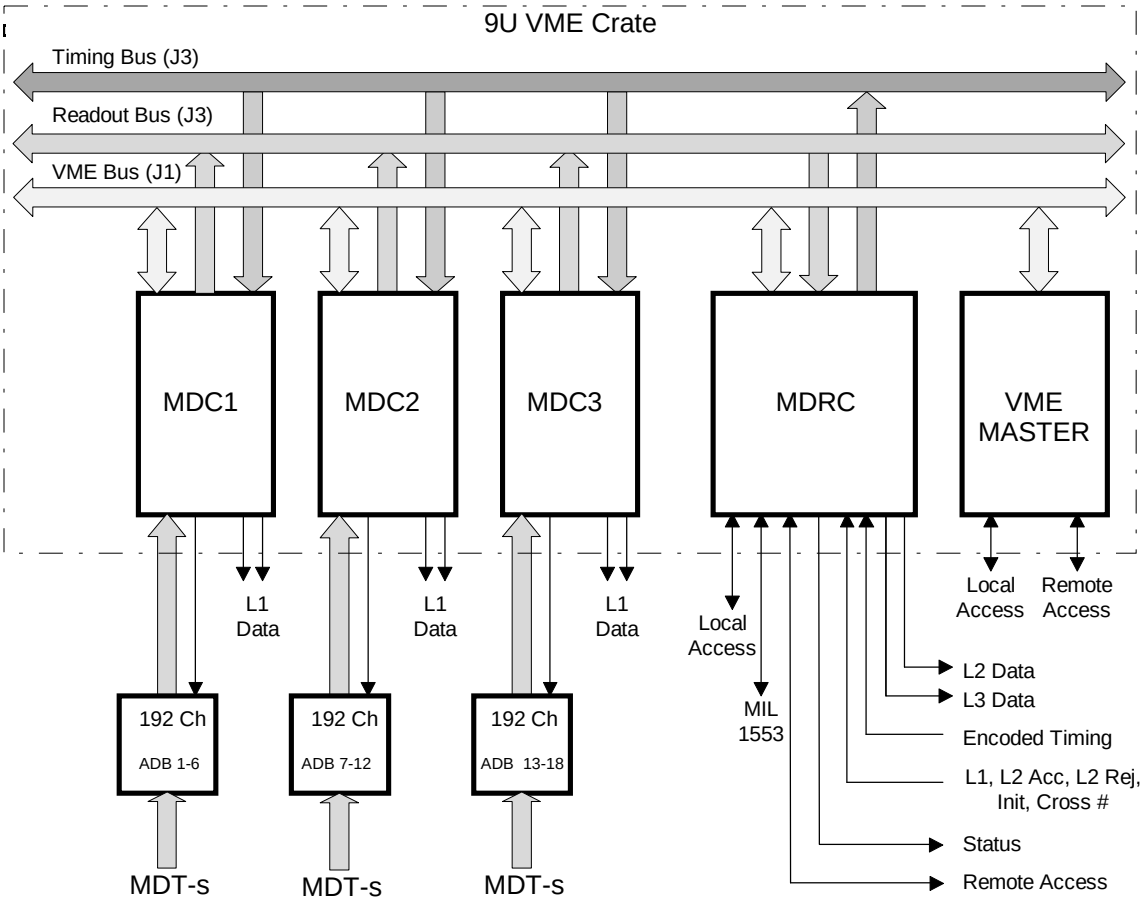



Fig. V-17. MDT front-end crate.

A serial control link provides an additional path to MIL-1553B for remote control and downloading during setup and run. A block-diagram of the MDRC in shown

Fig. V-18. The MDRC incorporates as many as four different functions: MDT Readout Controller, VME slave interface, MDT Communication Controller and MDT Monitor.

The MDRC as a Readout Controller performs the following functions:

- receives encoded timing signals [17,22] from the MRC, decode, trims them and passes them on to the MDCs over the Timing Bus

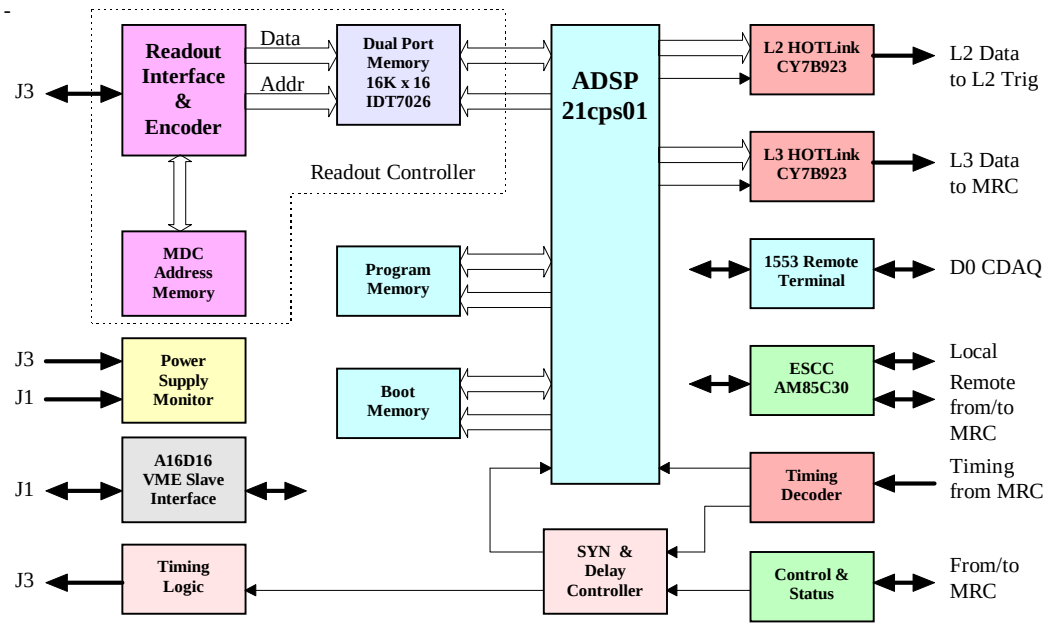



Fig. V-18. MDRC block-diagram.

- upon receiving an L1 Accept signal:
    1) passes the L1 Accept to all MDCs in the crate to store the corresponding event in the L1 FIFOs
    2) reads out stored data over the Readout Bus
    3) checks the validity of the data and send an error signal to the MRC if appropriate
    4) sparsifies and formats the data and writes it into the Dual Port Memory for later processing by the DSP
    5) sends out formatted data to the L2 Trigger over the L2 HOTLink at a 160 Mbit/sec rate
- upon receiving L2 Accept or L2 Reject signals either transmits data to the L3 over the HOTLink serial transmitter or discards it
- processes and reformats data in accordance with L3 requirements

The MDRC is an A16D16 VME Slave Interface with has access to all downloadable and readable registers and memories of the module

The MDRC as an MDT Communication Controller provides the following features:

- MIL 1553 Remote Terminal Interface
- Local and Remote Serial Interface based on the Am85C30 - Enhanced Serial Communications Controller chip

As an MDT Monitor the MDRC monitors the crate power supplies and temperature, and has comprehensive embedded MDC and ADB testing capabilities.

### C2. Mechanical Specification

The MDRC is a VME 9U by 280 mm card. It is assumed that each MDT crate constitutes a stand-alone readout station within the D0 detector and therefore has to have an AC outlet available on the platform. The MDRC uses its three backplane connectors for the following functions:

- **J1/J2** connections for standard VME operations
- custom **J3** connections for fast 64-bit wide data readout and for timing and control signals.

The rest of connectors are located on the front panel of the MDRC:

- A four conductor coaxial ribbon cable connector carrying:
  1) encoded timing information from MRC to MDRC;
  2) 53 MHz RF clock from MRC to MDRC;
  3) L2 Trigger Data from MDRC;
  4) L3 Data from MDRC;
- A 50-pin ribbon cable connector carrying:
  5) INIT from the MRC
  6) L1 Accept from the MRC
  7) L2 Accept and L2 Reject from the MRC
  8) Crossing # 0..7 from the MRC
  9) STRB and DONE from the MRC
  10) Remote Serial Interface to and from the MRC
  11) ERROR and BUSY from the MDRC to the MRC
- A MIL 1553 Serial Interface Connector Pair
- A Local Serial Interface Connector
- A Trigger Input and Trigger Output LEMO connectors for local triggering
- LEDs indicating module status

### C3. Timing Bus

The MDRC Timing Bus synchronizes the operation of all MDCs in the crate using a single accurately timed line (RF/7 = 7.58628 MHz) on the J3 backplane. All the rest of the timing signals (/First Crossing, /L1 Accept, /Gap, and /Test) are resynchronized by a falling edge of the RF/7 inside the MDCs (Fig. V-19). This approach has the following advantages:

- a lower reference clock frequency transmitted over the backplane
- the rest of the timing signals have longer setup and hold times for resynchronization

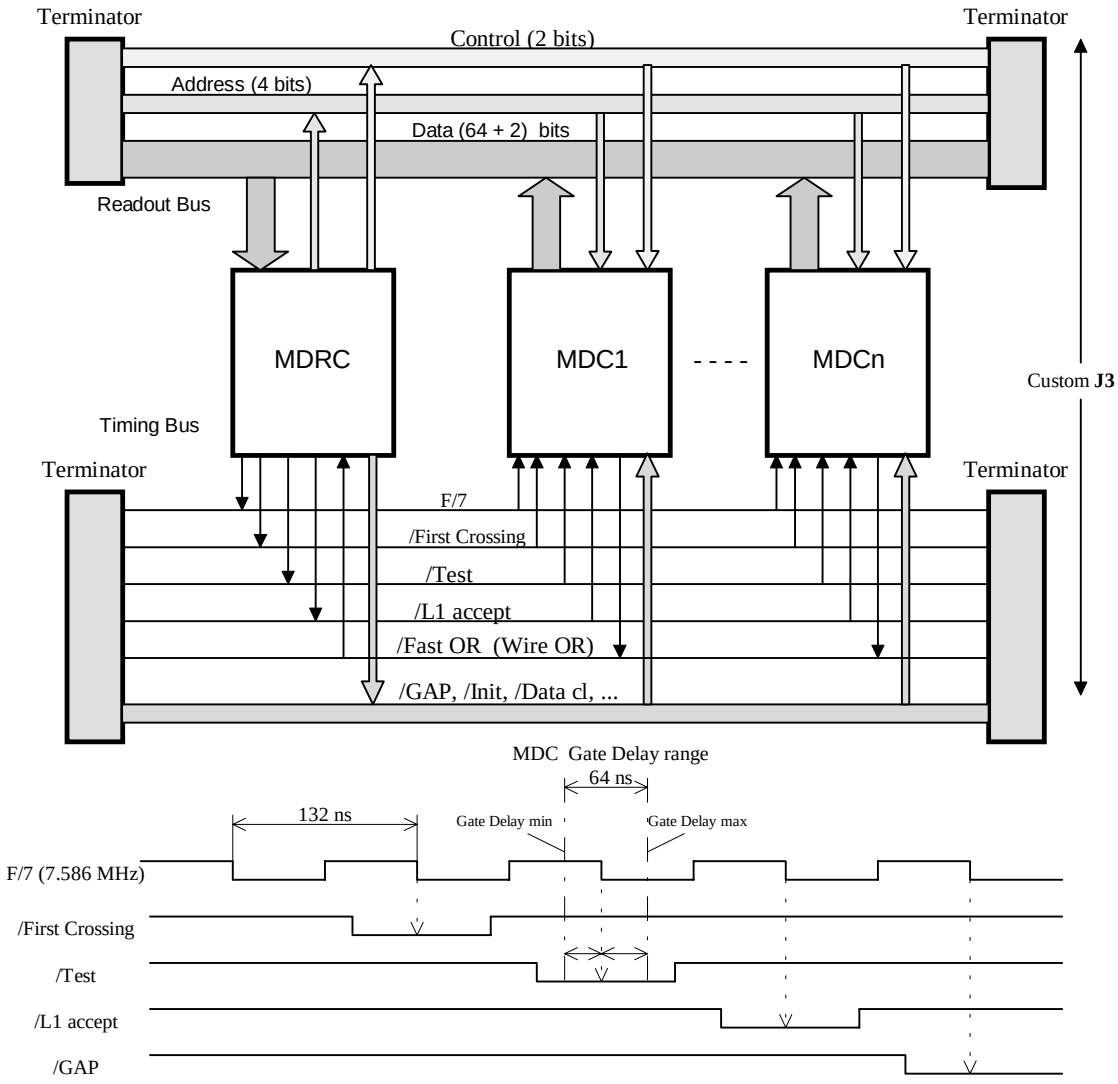



Fig. V-19. MDT readout and timing block-diagram.

## C4. Readout Controller

A block-diagram of the Readout Controller is shown in Fig. V-20. The Readout Controller performs the following functions:

- controls data readout from the MDCs and stores it in the Dual Port Memory, making it available for later DSP processing
- supports two modes of data processing:
    1) Sparse Mode: each hit is encoded into a separate 16-bit word while zeros are skipped, Table V-10
    2) Fixed Mode: a single bit carries a channel hit information and all channels are present at the output, Table **V-10.** Sparse Mode Data Format.

- calculates the Data Block Length of the processed data and writes it as a header at the beginning of the current block

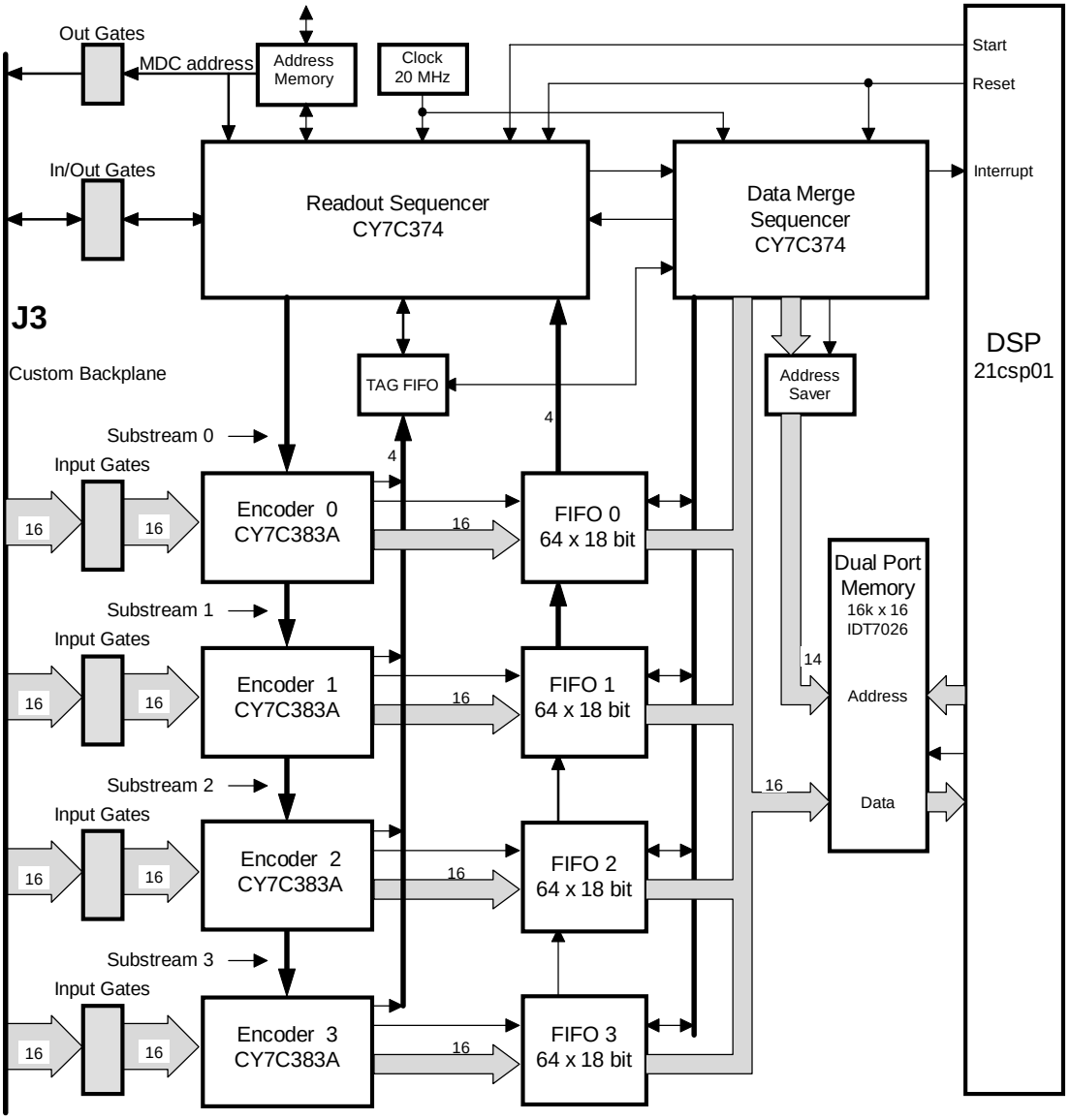



Fig. V-20. MDRC readout interface block-diagram.

To improve the throughput of the Readout Controller, the data stream is split into four Substreams, 16 bit wide, each feeding a separate encoder.

The encoder is implemented as a pipelined state machine, with an intrinsic processing latency of 300ns. While in Sparse Mode, the Readout Controller is capable of reading out and encoding at an 80Mbyte/s rate, if the number of hits in each 16-bit word is less than six. If this value is exceeded, each hit beyond six lengthens the readout process by 50ns. The encoder writes output data into a strobed FIFO. A dedicated Tag FIFO keeps track of

the number of occupied words in each substream. This information is used later by the Data Merge Sequencer.

The Data Merge Sequencer combines four Substreams into a single output which is written into the dual port memory, calculates the number of output data words and writes it as an event header. In the Sparse Mode all hits are sorted in ascending order. The number of data words in an event may vary from 0 to the number of MDCs in the crate times 192 (Table V-10). In Fixed Mode no sparsification or encoding is performed. The number of output words is constant and equals the number of MDCs in the crate times 12 (Table V-3). In this case, the readout rate is independent of the number of hits in MDCs and is fixed at 900 ns per MDC.

## Appendix A

### MDC SPECIFICATION

INPUT CONNECTORS

- Six 80-pin high density connectors,
- 32 ADB channels per connector
- 192 differential inputs terminated with 82 Ω resistors
- Minimum differential input voltage - 100 mV
- Nominal differential input voltage - 250 mV
- Minimum input signal width - 10 ns
- Differential Discriminator Level output voltage - -4.0V..+4.0V/10 kΩ
- Differential Test Pulse Level output voltage - -4.0V..+4.0V/10 kΩ
- Differential logic Test Pulse (current driver) - ±3.4 mA

OUTPUT CONNECTORS

- Two HF connectors for high speed serial links
- Fast OR output with NIM level signal (16mA/50 Ω)

INDICATORS

- Green LED , 20 ms flash per Fast OR pulse
- Yellow LED MDC Power OK
- Green LEDs VME access, MDRC access

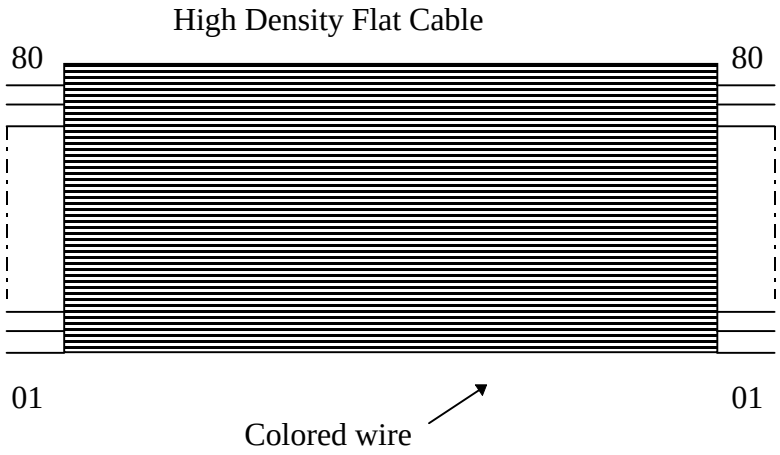
TIMING SIGNALS

- Reference clock RF/7 (supplied by the MDRC) - 7.58628 MHz
- Internal RF clock frequency (recovered in the MDC) - 53.103 MHz
- Gate Width range (GW) - 5..100 ns
  GW = 5 + N*9.41 ns, N=0..10
- Gate Delay range (GD) - 0..63 ns
  GD=N * 1 ns, N=0..63
- Drift time measurement bin width - 18.83 ns
- PipeLine Delay range (PD) - 0.13..8.3 us
  PD=N*0.132 μs, N=1..63
- Test Pulse Fine Delay range (TF) - 0..63 ns
  TF=N*1 ns, N=0..63
- Test Pulse Coarse Delay range (TC) - 0..282.4 ns
  TC=N*18.83 ns, N=0..15

# Appendix B.

## MDC CONNECTORS

Table V-5. MDC High Density Flat Cable Wire Assignment.




| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 80 | GND | 60 | +D09 | 40 | +D19 | 20 | +D29 |
| 79 | GND | 59 | - D09 | 39 | - D19 | 19 | - D29 |
| 78 | GND | 58 | +D10 | 38 | +D20 | 18 | +D30 |
| 77 | GND | 57 | - D10 | 37 | - D20 | 17 | - D30 |
| 76 | +D01 | 56 | +D11 | 36 | +D21 | 16 | +D31 |
| 75 | - D01 | 55 | - D11 | 35 | - D21 | 15 | - D31 |
| 74 | +D02 | 54 | +D12 | 34 | +D22 | 14 | +D32 |
| 73 | - D02 | 53 | - D12 | 33 | - D22 | 13 | - D32 |
| 72 | +D03 | 52 | +D13 | 32 | +D23 | 12 | GND |
| 71 | - D03 | 51 | - D13 | 31 | - D23 | 11 | GND |
| 70 | +D04 | 50 | +D14 | 30 | +D24 | 10 | Status |
| 69 | - D04 | 49 | - D14 | 29 | - D24 | 09 | Unassigned |
| 68 | +D05 | 48 | +D15 | 28 | +D25 | 08 | +Disc. Level |
| 67 | - D05 | 47 | - D15 | 27 | - D25 | 07 | - Disc. Level |
| 66 | +D06 | 46 | +D16 | 26 | +D26 | 06 | +Test Pulse Level |
| 65 | - D06 | 45 | - D16 | 25 | - D26 | 05 | - Test Pulse Level |
| 64 | +D07 | 44 | +D17 | 24 | +D27 | 04 | +Test Pulse |
| 63 | - D07 | 43 | - D17 | 23 | - D27 | 03 | - Test Pulse |
| 62 | +D08 | 42 | +D18 | 22 | +D28 | 02 | GND |
| 61 | - D08 | 41 | - D18 | 21 | - D28 | 01 | GND |

Table V-6. Level 1 Trigger Bit Assignment.

SERIAL LINK #1

Data bits:

| | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| word 1 | 091 | 085 | 079 | 073 | 067 | 061 | 055 | 049 | 043 | 037 | 031 | 025 | 019 | 013 | 007 | 001 |
| word 2 | 092 | 086 | 080 | 074 | 068 | 062 | 056 | 050 | 044 | 038 | 032 | 026 | 020 | 014 | 008 | 002 |
| word 3 | 093 | 087 | 081 | 075 | 069 | 063 | 057 | 051 | 045 | 039 | 033 | 027 | 021 | 015 | 009 | 003 |
| word 4 | 094 | 088 | 082 | 076 | 070 | 064 | 058 | 052 | 046 | 040 | 034 | 028 | 022 | 016 | 010 | 004 |
| word 5 | 095 | 089 | 083 | 077 | 071 | 065 | 059 | 053 | 047 | 041 | 035 | 029 | 023 | 017 | 011 | 005 |
| word 6 | 096 | 090 | 084 | 078 | 072 | 066 | 060 | 054 | 048 | 042 | 036 | 030 | 024 | 018 | 012 | 006 |
| | Input connector #3 Channels 065...096 | | | | | | Input connector #2 Channels 033...064 | | | | | Input connector #1 Channels 001...032 | | | | |

SERIAL LINK #2

Data bits:

| | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| word 1 | 187 | 181 | 175 | 169 | 163 | 157 | 151 | 145 | 139 | 133 | 127 | 121 | 115 | 109 | 103 | 097 |
| word 2 | 188 | 182 | 176 | 170 | 164 | 158 | 152 | 146 | 140 | 134 | 128 | 122 | 116 | 110 | 104 | 098 |
| word 3 | 189 | 183 | 177 | 171 | 165 | 159 | 153 | 147 | 141 | 135 | 129 | 123 | 117 | 111 | 105 | 099 |
| word 4 | 190 | 184 | 178 | 172 | 166 | 160 | 154 | 148 | 142 | 136 | 130 | 124 | 118 | 112 | 106 | 100 |
| word 5 | 191 | 185 | 179 | 173 | 167 | 161 | 155 | 149 | 143 | 137 | 131 | 125 | 119 | 113 | 107 | 101 |
| word 6 | 192 | 186 | 180 | 174 | 168 | 162 | 156 | 150 | 144 | 138 | 132 | 126 | 120 | 114 | 108 | 102 |
| | Input connector #6 Channels 161...192 | | | | | | Input connector #5 Channels 129...160 | | | | | Input connector #4 Channels 97...128 | | | | |

Table V-7. J1 Pin Assignment.

| Pin Number | Row A | Row B | Row C |
|---|---|---|---|
| 01 | D00 | *BBSY** | D08 |
| 02 | D01 | *BCLR** | D09 |
| 03 | D02 | *ACFAIL** | D10 |
| 04 | D03 | *BG0IN** | D11 |
| 05 | D04 | *BG0OUT** | D12 |
| 06 | D05 | *BG1IN** | D13 |
| 07 | D06 | *BG1OUT** | D14 |
| 08 | D07 | *BG2IN** | D15 |
| 09 | GND | *BG2OUT** | GND |
| 10 | *SYSCLK* | *BG3IN** | *SYSFAIL** |
| 11 | GND | *BG3OUT** | *BERR** |
| 12 | DS1* | *BR0** | SYSRESET* |
| 13 | DS0* | *BR1** | *LWORD** |
| 14 | WRITE* | *BR2** | AM5 |
| 15 | GND | *BR3** | *A23* |
| 16 | DTACK* | AM0 | *A22* |
| 17 | GND | AM1 | *A21* |
| 18 | *AS** | *AM2* | *A20* |
| 19 | GND | AM3 | *A19* |
| 20 | IACK* | GND | *A18* |
| 21 | *IACKIN** | *SERCLK* | *A17* |
| 22 | *IACKOUT** | *SERDAT** | *A16* |
| 23 | AM4 | GND | A15 |
| 24 | A07 | *IRQ7** | A14 |
| 25 | A06 | *IRQ6** | A13 |
| 26 | A05 | *IRQ5** | A12 |
| 27 | A04 | *IRQ4** | A11 |
| 28 | A03 | *IRQ3** | A10 |
| 29 | A02 | *IRQ2** | A09 |
| 30 | A01 | *IRQ1** | A08 |
| 31 | -12VDC | +5VDC | +12VDC |
| 32 | +5VDC | +5VDC | +5VDC |

*BBSY** - not used signals

Table V-8. J2 Pin Assignment.

| Pin Number | Row A | Row B | Row C |
|---|---|---|---|
| 01 | - | +5VDC | - |
| 02 | - | GND | - |
| 03 | - | *Reserved* | - |
| 04 | - | *A24* | - |
| 05 | - | *A25* | - |
| 06 | - | *A26* | - |
| 07 | - | *A27* | - |
| 08 | - | *A28* | - |
| 09 | - | *A29* | - |
| 10 | - | *A30* | - |
| 11 | - | *A31* | - |
| 12 | - | GND | - |
| 13 | - | +5VDC | - |
| 14 | - | *D16* | - |
| 15 | - | *D17* | - |
| 16 | - | *D18* | - |
| 17 | - | *D19* | - |
| 18 | - | *D20* | - |
| 19 | - | *D21* | - |
| 20 | - | *D22* | - |
| 21 | - | *D23* | - |
| 22 | - | GND | - |
| 23 | - | *D24* | - |
| 24 | - | *D25* | - |
| 25 | - | *D26* | - |
| 26 | - | *D27* | - |
| 27 | - | *D28* | - |
| 28 | - | *D29* | - |
| 29 | - | *D30* | - |
| 30 | - | *D31* | - |
| 31 | - | GND | - |
| 32 | - | +5VDC | - |

*A24* - not used signals

Table V-9. J3 Pin Assignment

| Pin Number | Row A | Row B | Row C |
|---|---|---|---|
| 01 | GNDA | GNDA | GNDA |
| 02 | F/7 | /Data_cl | GND |
| 03 | GND | /Init | /First_cross |
| 04 | /Spare1 | /GAP | GND |
| 05 | /L1_acc | /CLK | /Test |
| 06 | GND | /Fast_OR | /READ |
| 07 | /A0 | /A1 | /A2 |
| 08 | /A3 | /Last_Wd | /F_Err |
| 09 | /D_01 | /D_02 | /D_03 |
| 10 | /D_04 | /D_05 | /D_06 |
| 11 | GND | /D_07 | /D_08 |
| 12 | /D_09 | /D_10 | /D_11 |
| 13 | /D_12 | /D_13 | /D_14 |
| 14 | /D_15 | /D_16 | /D_17 |
| 15 | /D_18 | /D_19 | /D_20 |
| 16 | GND | /D_21 | /D_22 |
| 17 | /D_23 | /D_24 | /D_25 |
| 18 | /D_26 | /D_27 | /D_28 |
| 19 | /D_29 | /D_30 | /D_31 |
| 20 | /D_32 | /D_33 | /D_34 |
| 21 | GND | /D_35 | /D_36 |
| 22 | /D_37 | /D_38 | /D_39 |
| 23 | /D_40 | /D_41 | /D_42 |
| 24 | /D_43 | /D_44 | /D_45 |
| 25 | /D_46 | /D_47 | /D_48 |
| 26 | GND | /D_49 | /D_50 |
| 27 | /D_51 | /D_52 | /D_53 |
| 28 | /D_54 | /D_55 | /D_56 |
| 29 | /D_57 | /D_58 | /D_59 |
| 30 | /D_60 | /D_61 | /D_62 |
| 31 | GND | /D_63 | /D_64 |
| 32 | -5VDC | -5VDC | -5VDC |

Appendix C.

MDC VME REGISTERS

***CSR0***, Address 0XX0, Read/Write, Pipeline Delay and Gate Width Register,
unused bits read back as zeros

| 15 14 | 13 08 | 07 04 | 03 00 |
|---|---|---|---|
| | PD5 PD4 PD3 PD2 PD1 PD0<br>Pipeline Delay | | GW3 GW2 GW1 GW0<br>Gate Width |

***CSR1***, Address 0XX1, Write only, Initialization Register
bits 0..15 read back as zeros

| 15 03 | 02 | | 00 |
|---|---|---|---|
| | IR3<br>Clear | IR2<br>Reset | IR1<br>Init |

**Clear**, **Reset** and **Init** functions are performed by writing logical one to a corresponding bit.

**Init** - initializes Pipeline FIFO and L1 FIFO.
*Must be issued after any access to the register CSR0*;

**Clear** - initializes L1 FIFO;

**Reset** - loads following default values to the MDC registers:

| | | |
|---|---|---|
| PD | - Pipeline Delay | = 1 |
| GW | - Gate Width | = 10 |
| E001..E192 | | = 1 |
| TE1..TE8 | | = 1 |
| TF | - Test Fine Delay | = 0 |
| TC | - Test Coarse Delay | = 0 |
| GD | - Gate Delay | = 0 |
| TT | - Test Type | = 0 |

***CSR2***, Address 0XX2, Read/Write, Channel Enable Register,
bits are accessible by twelve sequential reads or writes to the same address.

| 15 03 | 02 00 |
|---|---|
| E016 E015 E014 E013 E012 E011 E010 E009 E008 E007 E006 E005 E004 | E003 E002 E001 |
| E032 ---------- | E017 |
| E048 ---------- | E033 |
| ⋮ | ⋮ |
| E176 ---------- | E161 |
| E192 ---------- | E177 |

***CSR3***, Address 0XX3, Read only, Error Status and ADB Status Register, unused bits read back as zeros

| 15 | 14 | | | 11 | 10 | 09 | | 06 | 05 | | | | | 00 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ES | PE4 | PE3 | PE2 | PE1 | IE | | | | AS6 | AS5 | AS4 | AS3 | AS2 | AS1 |
| Σ Err | Pipeline Error | | | | InitE | | | | ADB Status | | | | | |

ASx equals to "1" if a corresponding ADB is powered up and connected to the MDC.
ES - Error Status bit equals to a logical OR of the PE - Pipeline Error and IE - Init Error bits.

***CSR4***, Address 0XX4, Read/Write, Test Delay & Test Type Register, unused bits read back as zeros

| 15 | 12 | 11 | | | 08 | 07 | 06 | 05 | | | | | 00 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | TC3 | TC2 | TC1 | TC0 | TT | | TF5 | TF4 | TF3 | TF2 | TF1 | TF0 |
| | | Test Coarse Delay | | | | Type | | Test Fine Delay | | | | | |

TT - Test Type: TT=0 - Internal, TT=1 - External

***CSR5***, Address 0XX5, Read/Write, Gate Delay & Test Enable Register unused bits read back as zeros

| 15 | | | | | | | 08 | 07 | 06 | 05 | | | | | 00 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TE8 | TE7 | TE6 | TE5 | TE4 | TE3 | TE2 | TE1 | | | GD5 | GD4 | GD3 | GD2 | GD1 | GD0 |
| Test Enable | | | | | | | | | | Gate Delay | | | | | |

Test Enable bits control test signals depending on the status of the Test Type bit:

| Test Type / Test Enable Bit | TT=0 (Internal) | TT=1 (External) |
|---|---|---|
| TE1 | Ch001..Ch024 | ADB1 |
| TE2 | Ch025..Ch048 | ADB2 |
| TE3 | Ch049..Ch072 | ADB3 |
| TE4 | Ch073..Ch096 | ADB4 |
| TE5 | Ch097..Ch120 | ADB5 |
| TE6 | Ch121..Ch144 | ADB6 |
| TE7 | Ch145..Ch168 | |
| TE8 | Ch169..Ch192 | |

***CSR6,*** Address 0XX6, Write only, Discriminator Level Register

| 15 | | | | | | | 08 | 07 | | | | | | | 00 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | DL7 | DL6 | DL5 | DL4 | DL3 | DL2 | DL1 | DL0 |
| | | | | | | | | Discriminator Level | | | | | | | |

***CSR7,*** Address 0XX7, Write only, Test Pulse Level Register

| 15 | | | | | | | 08 | 07 | | | | | | | 00 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | TL7 | TL6 | TL5 | TL4 | TL3 | TL2 | TL1 | TL0 |
| | | | | | | | | Test Pulse Level | | | | | | | |

# Appendix D

## MDRC DATA READOUT MODES

Table V-10. Sparse Mode Data Format.

| 15 | | | | 11 | | | | | | | | | | | 00 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | L11 | L10 | L9 | L8 | L7 | L6 | L5 | L4 | L3 | L2 | L1 | L0 |
| | | | | Block Length | | | | | | | | | | | |

| 15 | 14 | | 12 | 11 | | | 08 | 07 | | | | | | | 00 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | T2 | T1 | T0 | M3 | M2 | M1 | M0 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| | Drift Time | | | MDC # | | | | Channel # | | | | | | | |

| | |
|---|---|
| | Block Length = 2 |
| | Data Word 1 |
| | Data Word 2 |
| | Block Length = 4 |
| | Data Word 1 |
| | Data Word 2 |
| | Data Word 3 |
| | Data Word 4 |
| | Block Length = 5 |
| | Data Word 1 |
| | Data Word 2 |
| | Data Word 3 |
| | Data Word 4 |
| | Data Word 5 |

Table V-11 Fixed Mode Data Format.

| 15 12 | 11 | | | | | | | | | | 00 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | L11 | L10 | L9 | L8 | L7 | L6 | L5 | L4 | L3 | L2 | L1 | L0 |
| | Block Length | | | | | | | | | | | |

| 15 | | | | | | | | | | | | | | | 00 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| H016 | H015 | H014 | H013 | H012 | H011 | H010 | H009 | H008 | H007 | H006 | H005 | H004 | H003 | H002 | H001 |
| Data Word Format (MDC Hits) | | | | | | | | | | | | | | | |

| | Block Length = (n x 12) |
|---|---|
| Data Word 1 (MDC1 channels 016-001) | |
| Data Word 2 (MDC1 channels 032-017) | |
| Data Word 3 (MDC1 channels 048-033) | |
| Data Word 4 (MDC1 channels 064-049) | |
| Data Word 5 (MDC1 channels 080-065) | |
| Data Word 6 (MDC1 channels 096-081) | |
| Data Word 7 (MDC1 channels 112-097) | |
| Data Word 8 (MDC1 channels 128-113) | |
| Data Word 9 (MDC1 channels 144-129) | |
| Data Word 10 (MDC1 channels 160-145) | |
| Data Word 11 (MDC1 channels 176-161) | |
| Data Word 12 (MDC1 channels 192-177) | |
| Data Word 13 (MDC2 channels 016-001) | |
| Data Word 14 (MDC2 channels 032-017) | |
| Data Word 15 (MDC2 channels 048-033) | |
| Data Word 16 (MDC2 channels 064-049) | |
| Data Word 17 (MDC2 channels 080-065) | |
| Data Word 18 (MDC2 channels 096-081) | |
| Data Word 19 (MDC2 channels 112-097) | |
| … | |
| … | |
| … | |
| Data Word (n x 12) (MDCn channels 192-177) | |

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